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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,178	01/30/2004	Arya Reza Behzad	BP 2475	7634

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EXAMINER	
NGUYEN, KHAI M	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 07/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/769,178	BEHZAD, ARYA REZA	
	Examiner	Art Unit	
	Khai M. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-9 and 12-14* is/are rejected.

7)☒ Claim(s) *5-6, 10-11, and 15-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 are pending. Claims 17-21 have been cancelled.

2. Claims 13 and 14 contain the same limitation. Clarification/correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Smith et al. (US 6,188,281). Smith et al. discloses (Figs. 6, 7A-C 8A-B, 10, 15-16) a DC coupled class AB transconductance block, comprising: first DC coupled transconductance stage (310) operably coupled to produce a first differential current (340) from a differential input voltage (330) based on a first bias voltage (first compensation circuit); second DC coupled transconductance stage (320) operably coupled to produce a second differential current (340) based on the differential input voltage (330) and a second bias voltage (the second compensation circuit), wherein output current of the class AB voltage current converter is a sum of the first differential current and the secondary differential current (the differential output current); and biasing circuit (the compensation circuits) operably coupled to produce the first bias voltage and the secondary bias

voltage, wherein the first bias voltage is greater than the secondary bias voltage (see column 3, lines 1-12 and Figs. 7A-7C).

4. Claims 1-4, 7-9, and 12-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Behzad et al. (US 6,496,067).

Regarding claim 1, Behzad et al. discloses (Fig. 5) a DC coupled class AB transconductance block, comprising: first DC coupled transconductance stage (12) operably coupled to produce a first differential current (20) from a differential input voltage (18) based on a first bias voltage (22); second DC coupled transconductance stage (14) operably coupled to produce a second differential current (24) based on the differential input voltage (18) and a second bias voltage (26), wherein output current of the class AB voltage current converter is a sum of the first differential current and the secondary differential current (output current 28); and biasing circuit (16) operably coupled to produce the first bias voltage and the secondary bias voltage, wherein the first bias voltage is greater than the secondary bias voltage.

Regarding claim 2, Behzad et al. discloses (Fig. 9) the first transconductance stage (12) further comprises: first DC coupled transistor (42 or 44) operably coupled to receive a combination of a first leg of the differential input voltage (Vin+ or Vin-) and the first bias voltage (Vref); and second DC coupled transistor (44 or 42) operably coupled to receive a combination of a second leg of the differential input voltage (Vin- or Vin+) and the first bias voltage (Vref – bias voltage 22), wherein the second transistor is operably coupled to the first transistor such that the first transistor produces a first leg of

the first differential current and the second transistor produces a second leg of the first differential current.

Regarding claim 3, Behzad et al. discloses (Fig. 10) the second transconductance stage (14) further comprises: first DC coupled transistor (46 or 48) operably coupled to receive a combination of a first leg of the differential input voltage (Vin+ or Vin-) and the secondary bias voltage (2^{nd} bias voltage 26); and second DC coupled transistor (48 or 46) operably coupled to receive a combination of a second leg of the differential input voltage (Vin- or Vin+) and the secondary bias voltage (bias voltage 26), wherein the second transistor is operably coupled to the first transistor such that the first transistor produces a first leg of the secondary differential current and the second transistor produces a second leg of the secondary differential current.

Regarding claim 4, Behzad et al. discloses the class AB voltage to current converter of claim 3 further including a third transconductance stage (see Fig. 12), the third transconductance stage further comprising: first DC coupled transistor operably coupled to receive a combination of a first leg of the differential input voltage and the secondary bias voltage; and second DC coupled transistor operably coupled to receive a combination of a second leg of the differential input voltage and the secondary bias voltage, wherein the second transistor is operably coupled to the first transistor such that the first transistor produces a first leg of the secondary differential current and the second transistor produces a second leg of the secondary differential current (see Figs. 9-11).

Regarding claim 7, Behzad et al. discloses the biasing circuit of claim 1 comprises a reference current source operably coupled to a current mirror to produce a bias signal (see 112 of Fig. 13).

Regarding claim 8, Behzad et al. discloses (Fig. 10) the biasing circuit of claim 1 comprises: first reference voltage source (58 or 60) operably coupled to produce the first bias voltage (22); second reference voltage source (60 or 58) operably coupled to produce the secondary bias voltage (26); first resistive pair (54/56) operably coupled to provide the first bias voltage to the first transconductance stage; and second resistive pair (74/76) operably coupled to provide the secondary bias voltage to the secondary transconductance stage.

Regarding claim 9, Behzad et al. discloses (see Fig. 12) the class AB voltage to current converter of claim 1 further comprises: third transconductance stage (102) operably coupled to produce a third differential current (104) based on the differential input voltage (18) and a third bias voltage (106), wherein output current of the class AB voltage current converter is the sum of the first differential current, the second differential current, and the third differential current, wherein the biasing circuit produces the third bias voltage, wherein the second bias voltage is greater than the third bias voltage (the first, second, and third bias voltages are imbalanced).

Regarding claim 12, Behzad et al. discloses (Fig. 10) a DC coupled class AB transconductance block, comprising: first DC coupled transconductance stage (12) operably coupled to produce a first differential current (20) from a differential input voltage (18) based on a first bias voltage (22); second DC coupled transconductance

stage (14) operably coupled to produce a second differential current (24) based on the differential input voltage (18) and a second bias voltage (26), wherein output current of the class AB voltage current converter is a sum of the first differential current and the secondary differential current (28); biasing circuit (16) operably coupled to produce a bias current; a resistor ladder comprising a plurality of resistors (54/56/72/74/76) wherein at least one resistor is electronically coupled between each transconductance stage of the DC coupled class AB transconductance block; wherein the first transconductance stage is biased to a different voltage level relative to the second transconductance stage; and wherein an output transconductance signal (28) is a sum of the transconductance signals produced by the first and second of the transconductance stages.

Regarding claims 13-14, Behzad et al. discloses the DC coupled class AB transconductance block of claim 12 further comprising a third transconductance stage (102 – Fig. 12).

5. Regarding claims 5-6, 10-11, and 15-16, these claims are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Prior Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclose (see references cited on PTO-892 Form attached herewith).

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khai M. Nguyen whose telephone number is 571-272-1809. The examiner can normally be reached on 9:00 - 5:30 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert (Bob) J. Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KN
July 6, 2005

PEGUY JEANPIERRE
PRIMARY EXAMINER